Q.P. Code:**16EC5702** **R16**

Reg. No. | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
M.Tech I Year I Semester Regular & Supplementary Examinations February 2018
ANALOG IC DESIGN
(VLSI)

Time: **3 hours** Max. Marks: **60**

(Answer all Five Units **5 X 12 =60** Marks)

UNIT-I

1	a	Explain the operation of simple CMOS current mirror.	7M
	b	Explain the effect of threshold voltage on MOSFET current equations.	5M
		OR	
2	a	Explain briefly large signal modeling for BJT with basic current mirrors	7M
	b	What are the deficiencies of MOS technology? How they can it be overcome.	5M

UNIT-II

3	a	Discuss the various short channel effects in MOS devices.	5M
	b	Explain the terms stability, frequency compensation and phase margin in op-amp.	7M
		OR	
4	a	Explain in detail about current feedback OP-amplifier..	7M
	b	Explain latched comparators.	5M

UNIT-III

5	a	Compare the design aspects of MOS, CMOS and BICMOS sample and hold circuit	7M
	b	Explain the correlated double sampling techniques with suitable example..	5M
		OR	
6	a	Discuss the different performance characteristics of sample/hold circuits.	7M
	b	Explain about Switched capacitor gain circuit.	

UNIT-IV

7	a	Explain the operation of over sampling A/D converter.	5M
	b	Explain the design procedure for integrates A/D converters.	7M
		OR	
8	a	Explain the working of a Hybrid DAC.	7M
	b	Explain in detail about Ideal D/A & A/D converters.	5M

UNIT-V

9	a	Explain the structure of a first order noise shaped sigma delta modulator.	7M
	b	How does noise shaping improve the signal to noise ratio.	5M
		OR	
10	a	Discuss about Continuous time filters.	5M
	b	Explain about Over sampling with Noise shaping.	7M

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